# Multilevel Sub-modeling Study of Packaging Effects on Mechanical Reliability of Cu/low k Chips

Paul S. Ho

Microelectronics Research Center, University of Texas at Austin, TX 78712

## Abstract

With continuing device scaling, copper interconnects integrated with low k dielectrics are implemented in advanced high-performance microprocessor chips. For Cu/low k chips, chip-packaging interaction is becoming a critical reliability issue when they are assembled into plastic flip-chip packages. In a flip-chip package, the thermal deformation of the package can be directly coupled into the Cu/low k interconnect structure inducing large local deformation to drive interfacial crack formation. This paper will summarize the experimental and modeling studies to investigate the chip-package interaction and its impact on low k interconnect reliability. First, the packaging induced deformation and stress at the chip level is analyzed using high-resolution moiré interferometry and compared with process-induced stresses during chip fabrication. Then results from 3D finite element analysis (FEA) based on a multilevel sub-modeling approach to investigate the chip-package interaction for low k interconnects will be presented. Packaging induced crack driving forces for relevant interfaces in Cu/low k structures are deduced and compared. Their effects on packaging reliability will be discussed.